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Abstract
In the last decade, discrete wavelet transform (DWT) has proven to be a useful technique for a wide rage of application including signals analysis, signal compression, pattern recognition, biomedicine, and numerical analysis. Since DWT has excellent features of energy compaction and inherent scalability, it has been applied extensively in the field of image and video compression. The traditional DWT needs extensive computation complexity. In 1996, Lifting-Based Discrete Wavelet Transform (LDWT), is proposed. With some advantages, such as lower implementation complexity and easy VLSI implementation, LDWT has received considerable attention recently and been adopted in some image compression standards.

We propose a very flexible soft LDWT IP generator in this thesis. With the help of the auxiliary software interface, users can choose easily different LDWT architectures (5/3 or 9/7), dimensions (1-D or 2-D), levels (1 to 5), and transforms (forward and inverse). Because of the excellent flexibility, the proposed LDWT IP is very suitable for various real-time DWT applications.

The design has been synthesized on Synopsys Design Compiler with the standard-cell from UMC 0.18-μm cell library. Finally, the layout for the design was generated with the Avant! tools, Apollo (for floorplan, placement and routing), and Dracula (for DRC, ERC and LVS checks). It core size and gate count are about 1.535*1.531 mm2 and 13732.7, respectively for 9/7 2-D 3-L forward LDWT. In the simulation, it’s clock frequency achieves 131. 2MHz.
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